IN THE CLAIMS

1. (Currently amended) A capacitor formed on a semiconductor substrate, the capacitor comprising:

a first electrode of a first metal layer;

a second electrode of a second metal layer that is closer to the substrate than the first metal layer;

a dielectric material intermediate the first and second electrodes; and

a wire coupled to a bottom surface of the first electrode,

wherein the first electrode is coupled to the wire through a contact hole in the dielectric material.

2. (Original) The capacitor of claim 1 wherein the wire is formed of a third metal layer that is closer to the substrate than the second metal layer.

3. (Original) The capacitor of claim 1 wherein the wire is formed of the second metal layer.

4. (cancelled)

5. (Original) The capacitor of claim 4 wherein the contact hole comprises a plurality of separate contact holes.

6. (Original) The capacitor of claim 1 wherein the wire has a planarized top surface.

7. (Original) The capacitor of claim 6 wherein the wire comprises a damascene layer.

8. (Currently amended) A metal-insulator-metal capacitor, comprising:

a wire layer formed in a first metal layer, the wire layer including a first electrode contacting line;

a bottom electrode formed in a second metal layer;

a top electrode formed in a third metal layer, the top electrode disposed over the bottom electrode;

a dielectric layer separating the bottom electrode from the top electrode; ~~and~~

a contact formed between the first electrode contacting line and a bottom side of the top electrode; and

a second contact located on a top side of the bottom electrode.

9. (Original) The capacitor of claim 8 wherein the top electrode couples to the first electrode contacting line through a contact hole in the dielectric layer.

10. (Original) The capacitor of claim 9 wherein the contact hole comprises a plurality of separate holes.

11. (Original) The capacitor of claim 8, wherein the wire layer comprises a second electrode contacting line, and wherein the second electrode contacting line is coupled to a bottom surface of the bottom electrode.

12. (Original) The capacitor of claim 11, wherein a portion of the bottom surface of the bottom electrode directly contacts a top surface of the second electrode contacting line and not through a contact hole.

13. (Original) The capacitor of claim 11 wherein the bottom electrode couples to the second electrode contacting line through a contact hole in an insulation layer.

14. (Original) The capacitor of claim 11 wherein the first and second electrode contacting lines each have a planarized top surface.

15. (Original) The capacitor of claim 14 wherein the first and second contacting lines are planarized by a damascene process.

16. (Original) The capacitor of claim 14 wherein the first and second contacting lines are planarized by a CMP process performed on an interlayer dielectric layer.

17. (Original) The capacitor of claim 11 wherein a top surface of the first and second contacting lines are formed in a process other than planarization.

18. (cancelled)

19. (Original) The capacitor of claim 18, wherein the second contact extends away from the substrate farther than the third metal layer.

20. (Currently amended) A metal-insulator-metal capacitor, comprising:

a first metal layer including a bottom electrode and an electrode contacting line;

a top electrode formed in a second metal layer, the top electrode disposed over the bottom electrode;

a dielectric layer separating the bottom electrode from the top electrode; ~~and~~

a contact formed between the electrode contacting line and a bottom side of the top electrode; and

a second contact located on a top side of the bottom electrode.

21. (Original) The capacitor of claim 20 wherein the top electrode couples to the electrode contacting line through a contact hole in the dielectric layer.

22. (Original) The capacitor of claim 21 wherein the contact hole comprises a plurality of separate holes.

23. (cancelled)

24. (Original) The capacitor of claim 23, wherein the second contact extends away from the substrate farther than the second metal layer.

25. (Original) The capacitor of claim 20 wherein the bottom electrode and the electrode contacting line each have a planarized top surface.

26. (Original) The capacitor of claim 25 wherein the bottom electrode and the electrode contacting line are planarized by a damascene process.

27. (Original) The capacitor of claim 25 wherein the bottom electrode and the electrode contacting line are planarized by a CMP process performed on an interlayer dielectric layer.

28. (Original) The capacitor of claim 20 wherein the bottom electrode and the electrode contacting line are formed in a process other than planarization.

29-51 (cancelled).

52. (New) A metal-insulator-metal capacitor, comprising:

a wire layer formed in a first metal layer, the wire layer including a first electrode contacting line;

a bottom electrode formed in a second metal layer;

a top electrode formed in a third metal layer, the top electrode disposed over the bottom electrode;

a dielectric layer separating the bottom electrode from the top electrode; and

a contact formed between the electrode contacting line and a bottom side of the top electrode, wherein the top electrode couples to the first electrode contacting line through a contact hole in the dielectric layer.